Freescale Semiconductor
Application Note

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Design Checklist for PowerQUICC II Pro MPC8308 Processor

This application note describes the generally recommended connections for new designs based on the Freescale MPC8308 processor. The design checklist may also apply to future bus or footprint-compatible processors. It can also serve as a useful guide for debugging a newly-designed system, by highlighting those areas of a design that merit special attention during initial system startup.

Contents

1 MPC8308 Background

This section outlines recommendations to simplify the first phase of design. Before designing a system with a PowerQUICC™ II Pro device, the designer should be familiar with the available documentation, software, models, and tools.

1.1 References

Some references listed here may be available only under a nondisclosure agreement (NDA). Contact your local field applications engineer or sales representative to obtain a copy.

- Collateral
  - — *MPC8308 PowerQUICC II Pro Processor Reference Manual* (MPC8308RM)
  - — *MPC8308 Chip Errata* (MPC8308CE)
  - — *MPC8308 PowerQUICC II Pro Processor Hardware Specification* (MPC8308EC)
- Models
  - — IBIS
  - — BSDL

1.2 Device Errata

The device errata document (MPC8308CE) describes the latest fixes and workarounds for MPC8308. Carefully study this document before starting a design with MPC8308.

1.3 Product Revision

This table lists the PowerQUICC II Pro (MPC8308) product revision.

Table 1. PowerQUICC II Pro (MPC8308) Product Revision

Device	Package	SVR (Rev. 1.0)	PVR (Rev. 1.0)
MPC8308	473-MAPBGA	8101_0010	8085_0020

2 Power

This section provides design considerations for the PowerQUICC II Pro power supplies, as well as power sequencing. For information on PowerQUICC II Pro AC and DC electrical specifications and thermal characteristics, refer to MPC8308EC. For power sequencing recommendations, see Section 2.2, "Power Consumption."

2.1 Power Supply

The PowerQUICC II Pro has a core voltage, V_{DD}, that operates at a lower voltage than the I/O voltages GV_{DD}, LV_{DD}, and NV_{DD}.The V_{DD} should be supplied through a variable switching supply or regulator to allow for compatibility with core voltage changes on future silicon revisions. The core voltage, 1.0 V (±5%), is supplied across V_{DD} and GND.

The MPC8308EC lists the recommended range for each power supply listed in Table 2. These voltages are typically supplied by simple linear regulators, which increases the complexity of the system because multiple voltage supplies and PCB power planes are required for the design. No external signals on the MPC8308 are 5-V-tolerant. Note that absolute maximum ratings are stress ratings only. The functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or permanently damage the device.

2.2 Power Consumption

The MPC8308EC provides the power dissipation of V_{DD} for various configurations of the coherent system bus (CSB) and the e300 core frequencies. The hardware specification also estimates power dissipation for all the I/O power rails. I/O power highly depends on the application and is an estimate. A full analysis of board implementation is required to define I/O power supply needs. The typical V_{DD} power plus I/O power should be used for the thermal solution design. The junction temperature should not exceed the maximum specified value. The maximum V_{DD} power is the worst case power consumption and should be used for the core power supply design.

2.3 Power Sequencing

One consequence of multiple power supplies is that when power is initially applied, the voltage rails ramp up at different rates. These rates depend on the power supply, the type of load on each power supply, and the manner in which different voltages are derived. However, advances in the PowerQUICC II Pro ESD design allow flexibility in the order in which power rails ramp up, as long as the supplies do not exceed absolute maximum ratings (as defined in the MPC8308EC).

NOTE

From a system standpoint, if the I/O power supplies ramp up before the V_{DD} core supply stabilizes there may be a period of time when the I/O pins are driven to a logic one or logic zero state. After the power is stable, as long as $\overline{\text{PORESET}}$ is asserted, most IP pins are three-stated. To minimize the time that I/O pins are actively driven, apply core voltage before I/O voltage and assert $\overline{\text{PORESET}}$ before the power supplies fully ramp up.

Table 2 lists the recommended operating voltages for the power supplies. Note that supplies must not exceed these absolute maximum ratings. However, during normal operation, use of the recommended operating conditions tables (as in *PowerQUICC II Pro MPC8308 Hardware Specification*) is recommended. Any information in the relevant hardware specifications supersedes information in Table 2.

This figure shows a power sequencing example.

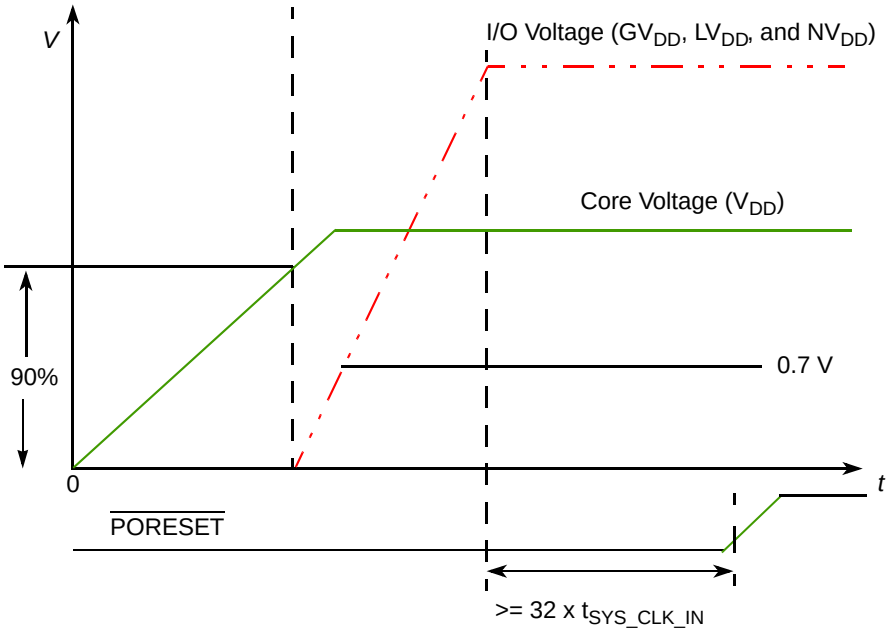


Figure 1. Power Sequencing Example

2.4 Power Planes

Each V_{DD} pin should be provided with a low-impedance path to the board power supply. Similarly, each ground pin should be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on-chip. The capacitor leads and associated printed-circuit traces connecting to chip V_{DD} and ground should be kept to less than half an inch per capacitor lead.

2.5 Decoupling

Due to large address/data buses and high operating frequencies, the PowerQUICC II Pro can generate transient power surges and high-frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the PowerQUICC II Pro system, and it requires a clean, tightly regulated source of power. Therefore, the system designer should place at least one decoupling capacitor at each V_{DD}, GV_{DD}, LV_{DD} , and NV_{DD} pin. These decoupling capacitors should receive their power from separate V_{DD}, GV_{DD}, LV_{DD}, NV_{DD}, and GND power planes in the PCB, using short traces to minimize inductance. Capacitors can be placed directly under the device using a standard escape pattern. Other capacitors can surround the part. These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic surface mount technology (SMT) capacitors should be used to minimize lead inductance.

In addition, several bulk storage capacitors should be distributed around the PCB, feeding the V_{DD}, GV_{DD}, LV_{DD}, and NV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low equivalent series resistance (ESR) rating to ensure quick response time. They should also connect to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors: 100–300 µF.

Use simulation to minimize noise on the power supplies before proceeding into the PCB design and manufacturing stage of development.

2.6 PLL Power Supply Filtering

Each PowerQUICC II Pro PLL gets power through independent power supply pins (AV_{DD1} and AV_{DD2}). The AV_{DD} level should be derived directly from V_{DD} through a low frequency filter scheme.

There are several reliable ways to provide power to the PLLs, but the recommended solution is to use independent filter circuits as illustrated in Figure 2, one to each of the AV_{DD} pins, thus reducing noise injection from one PLL to the other. This circuit filters noise in the PLL resonant frequency range from 500 KHz to 10 MHz. It should be built with surface mount capacitors with a minimum effective series inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended instead of a single large value capacitor.

Place each circuit as closely as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin without the inductance of vias.

This figure shows the PLL power supply filter circuit for CORE PLL(AV_{DD1}) and SYSTEM PLL(AV_{DD2}).

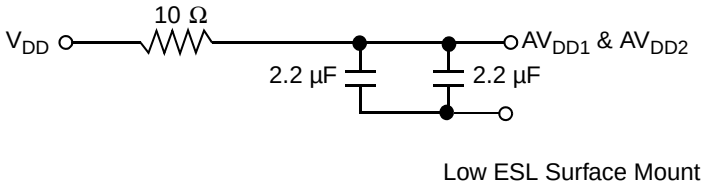


Figure 2. PLL Power Supply Filter Circuit

This figure shows the PLL power supply filter circuit for SERDES PLL (SDAVDD).

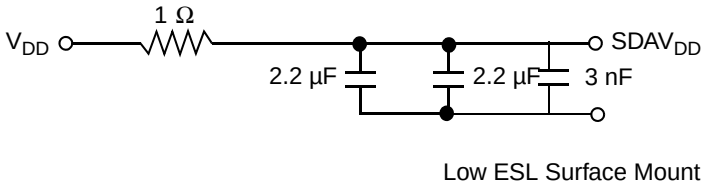


Figure 3. SERDES PLL Power Supply Filter Circuit

3 Pin Listing and Connections

This table summarizes the power signal pins.

Table 2. Power Signal Pin Listing

Signal	Connection	Notes
AV_{DD1}	1.0 V ± 50 mV	Analog power for e300 core PLL
AV_{DD2}	1.0 V ± 50 mV	Analog power for system PLL
SDAVDD	1.0 V ± 50 mV	SerDes analog power for PLL
GV_{DD}	1.8 V ± 100 mV	DDR2 I/O voltage
MVREF	0.49xGV_{DD} to 0.51 xGV_{DD}	DDR2 reference voltage
LV_{DD}	2.5 V ± 125 mV or 3.3 V ± 300 mV	eTSEC1/eTSEC2 I/O supply
V_{DD}	1.0 V ± 50 mV	Core supply voltage
NV_{DD}	3.3 V ± 300 mV	Standard I/O voltage
XCOREVDD	1.0 V ± 50 mV	SerDes internal digital power
XPADVDD	1.0 V ± 50 mV	SerDes I/O digital power

NOTE

All the power pins must be tied to their corresponding voltages irrespective of the fact that a module is used or not in the system. For example, even if PCI Express interface is not used in the system, the PCI Express power pins (SDAVDD, XPADVDD, and XCOREVDD) must be tied to their corresponding voltages.

4 Clocking

This figure shows the internal distribution of clocks within the MPC8308.

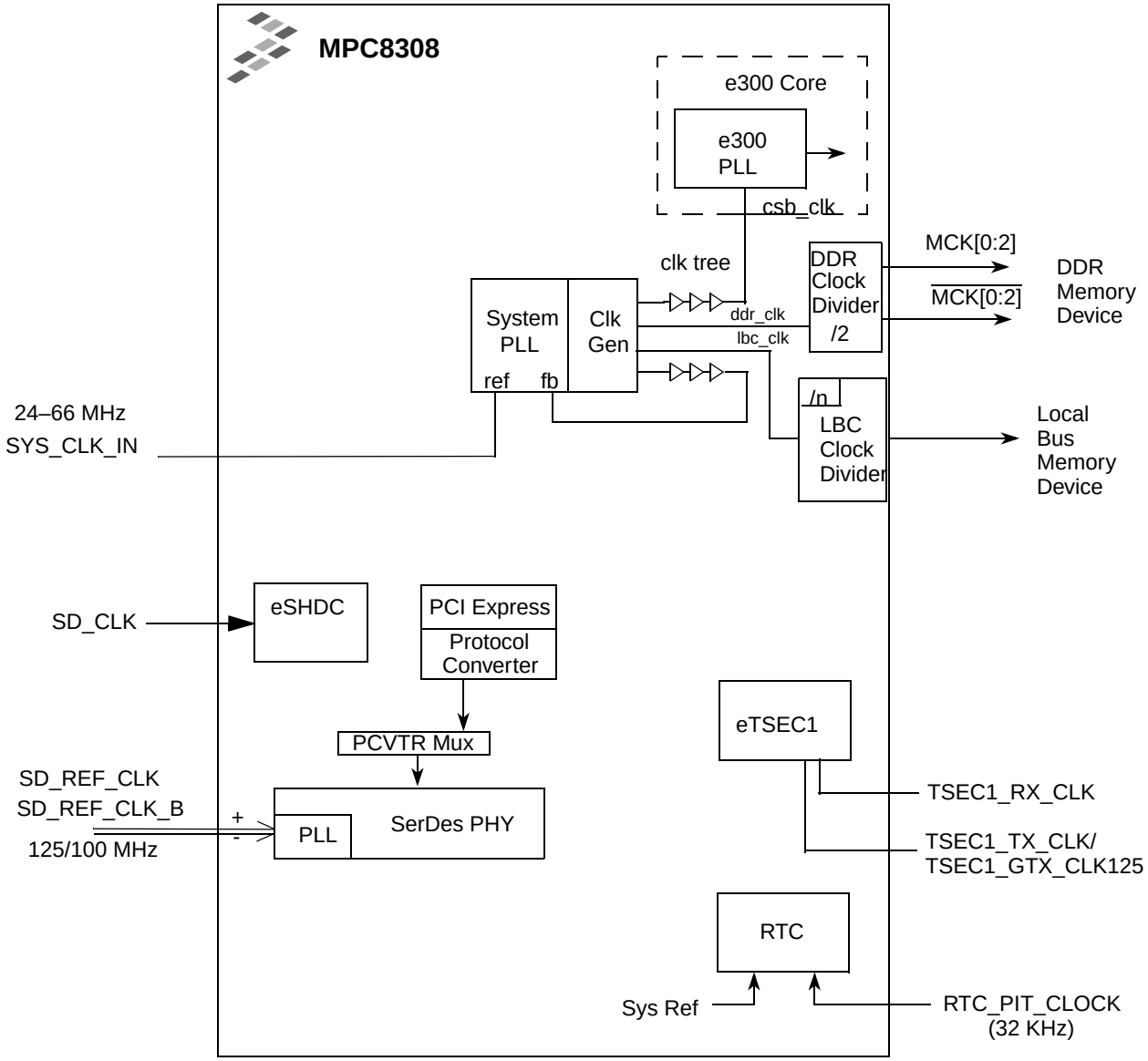


Figure 4. Clock Subsystem Block Diagram

This table lists the clock signal pins.

Table 3. Clock Signal Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
SYS_CLK_IN	I	Connect to 24–66.66 MHz clock signal (Recommended: 33MHz)	Not applicable	A valid 24–66.66 MHz clock signal (at NV_{DD} level) must be applied to this input when used.
TSEC*n*_GTX_CLK125	I	Connect to 125 MHz clock signal	1 k–4.7 kΩ to GND	In the RGMII mode, a valid 125 MHz clock signal must be applied to this signal. This must be externally generated with an oscillator or provided by the PHY.
$\overline{\text{SD\_REF\_CLK}}$/ SD_REF_CLK (PCI Express PHY Clock)	I	Connect to a 100 MHz differential clock for PCI Express	Tie both the pins to GND	A Valid 100 MHz clock signal must be applied to this input when used. The reference is 1 V and not 3.3 V.
RTC_PIT_CLOCK	I	Connect to clock signal	Connect to clock signal if RTC block is used. 1 k–4.7 kΩ to GND if RTC block is not used.	Refer to Erratum A-003985 in MPC8308 Chip Errata document (MPC8308CE), Rev. 1 or later.

4.1 System Clock

The primary clock source for the MPC8308 is provided at the SYS_CLK_IN pin. This is typically provided by a crystal oscillator in the frequency range of 24–66 MHz. The recommended value is 33 MHz.

4.2 PCI Express Clocking

The MPC8308 processor contains an integrated PHY that can be programmed to act as a PCI Express lane. This PHY has its own PLL and requires a 100 MHz differential clock reference input. The reference is 1 V and not 3.3 V. The PHY generates its own transmit and receive sampling clock. The receive clock is recovered from the receive data. The PHY supplies the transmit/receive clock between the PHY and the MAC (PCI Express controller). Synchronization between the MAC and the CSB clock domain occurs in the MAC. For proper synchronization, the CSB must be running at a higher frequency than the transmit/receive clock.

4.3 eTSEC Clocking

In the RGMII mode, TSEC1_GTX_CLK125 and TSEC2_GTX_CLK125 require a 125 MHz clock signal. In the MII mode, these signals are unused.

5 Power-On Reset and Reset Configurations

A detailed power-on reset flow is as follows:

1. Power to the device is applied.
2. The system asserts $\overline{\text{PORESET}}$ (and optionally $\overline{\text{HRESET}}$) and $\overline{\text{TRST}}$ initializing all registers to their default states.
3. The system applies a stable SYS_CLK_IN signal and stable reset configuration inputs (CFG_RESET_SOURCE).
4. The system negates $\overline{\text{PORESET}}$ after at least 32 stable SYS_CLK_IN clock cycles.
5. The device samples the reset configuration input signals to determine the reset configuration words source.
6. The device starts loading the reset configuration words. When the reset configuration word low is loaded, the system PLL begins to lock. When the system PLL is locked, the *csb_clk* is supplied to the e300 PLL.
7. The e300 PLL begins to lock.
8. The device drives $\overline{\text{HRESET}}$ asserted until the e300 PLL is locked and until the reset configuration words are loaded.
9. If enabled, the boot sequencer loads configuration data from the serial EEPROM as described in the *MPC8308 PowerQUICC II Pro Processor Reference Manual*. The configuration data can also be loaded from NOR/NAND Flash.

5.1 Reset Configuration Signals

Various device functions of the PowerQUICC II Pro are initialized by sampling certain signals during the assertion of the $\overline{\text{PORESET}}$ signal after a stable clock is supplied. These inputs are either pulled high or low. Although these pins are generally output pins during normal operation, they are treated as inputs while $\overline{\text{PORESET}}$ is asserted. See this table for termination recommendations for the reset configuration pins.

Table 4. Reset Configuration Pin Listing

Signal	Pin Type	Termination
$\overline{\text{PORESET}}$	I	Driven actively by the external reset logic
$\overline{\text{HRESET}}$	I/O	Pullup with 1.5 kΩ to NV_{DD}
TSEC1_TXD3/ CFG_RESET_SOURCE0	I/O	Pull up with 4.7 kΩ to LV_{DD} or pull down with 1 kΩ to GND as desired, see Table 5 OR Driven as needed during $\overline{\text{HRESET}}$ assertion and tri-state after HRESET negation The length of the stubs introduced by connecting the resistors or any other active device should be kept minimum. Failing to do so may distort the TSEC1 transmit data signals.
TSEC1_TXD2/ CFG_RESET_SOURCE1	I/O	
TSEC1_TXD1/ CFG_RESET_SOURCE2	I/O	
TSEC1_TXD0/ CFG_RESET_SOURCE3	I/O	
TSEC1_TX_ER/ LB_POR_CFG_BOOT_ECC	I/O	Pull up with 1.5K kΩ to LV_{DD}; no pull down resistor required when logic 0 needs to be driven as the internal pull down is implemented in SOC OR Driven as needed during $\overline{\text{HRESET}}$ assertion and tri-state after HRESET negation.
TSEC1_TX_EN/ LBC_PM_REF_10	O	LBC_PM_REF_10 indicates if local bus RCW load failed during HRESET assertion period.

For the TSEC1_TX_ER/LB_POR_CFG_BOOT_ECC signals, this figure shows the circuit to disable ECC checking during boot-up.

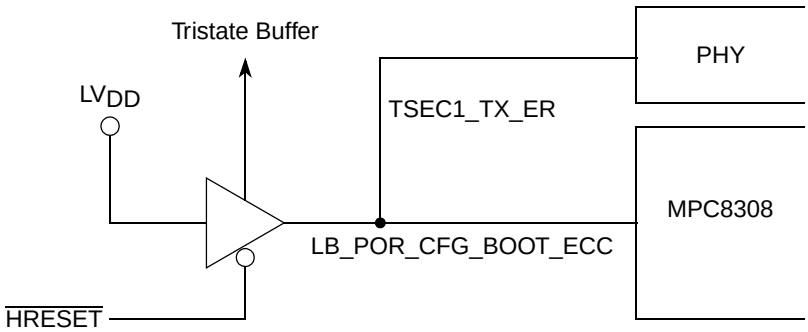


Figure 5. Recommended Circuit for Disabling ECC Checking during Boot-Up

The CFG_RESET_SOURCE[0:3] input signals are sampled during the assertion of $\overline{\text{PORESET}}$ to select the interface to load the reset configurations words:

- I^2C interface
- A device (that is, CPLD, EEPROM, or NOR/NAND Flash) on the local bus
- From a hard-coded value

For more information, see *MPC8308 PowerQUICC II Pro Processor Reference Manual*.

5.2 Reset Configuration Words

The reset configuration words control the clock ratios and other basic device functions such as, boot location, eTSEC modes, and endian mode. The reset configuration words are loaded from the local bus or from the I^2C interface during the power-on or hard reset flows. If the reset configuration word is from the flash memory, it should reside at the beginning of the flash memory. That is, it should start from address 0. A total of two 32-bit-words are read. The first byte is read from address 0x0, the second byte from address 0x8, the third byte from address 0x10, and so on until all 8 bytes are read. Bytes b0–b3 form a word, and this is the reset configuration word low register (RCWLR). Bytes b4–b7 form the reset configuration word high register (RCWHR). For more information, see the "Reset, Clocking, and Initialization" chapter from *MPC8308 PowerQUICC II Pro Processor Reference Manual*.

- RCWLR
  0x0000: b0xxxxxx xxxxxxxx
  0x0008: b1xxxxxx xxxxxxxx
  0x0010: b2xxxxxx xxxxxxxx
  0x0018: b3xxxxxx xxxxxxxx
- RCWHR
  0x0020: b4xxxxxx xxxxxxxx
  0x0028: b5xxxxxx xxxxxxxx
  0x0030: b6xxxxxx xxxxxxxx
  0x0038: b7xxxxxx xxxxxxxx

If the reset configuration word is from an I^2C device, the I^2C setup must comply with the following requirements:

- EEPROM of extended address type must be used.
- EEPROM must respond to the calling address 0x101_0000.
- Use the special data format as described in *MPC8308 PowerQUICC II Pro Processor Reference Manual*.

5.3 Useful System POR Debug Registers

The hardware reset configuration settings can be read in the reset configuration word low register (RCWLR), the reset configuration word high register (RCWHR), the reset status register (RSR), and the system PLL mode register (SPMR). For more information, see *MPC8308 PowerQUICC II Pro Processor Reference Manual*. Note that all of these registers are read-only, except RSR.

5.4 Boot Sequencer

The boot sequencer provides the means to load the hardware reset configuration word and to configure any memory-mapped register before the boot-up code runs. Reset configuration load mode is selected based on the settings of the CFG_RESET_SOURCE pins during the power-on reset sequence. The I^2C interface loads the reset configuration words from an EEPROM at a specific calling address while the rest of the

device is in the reset state. When the reset configuration words are latched inside the device, I^2C is reset until $\overline{\text{HRESET}}$ is negated. Then the device is initialized using boot sequencer mode.

Boot sequencer mode is selected at power-on reset by the BOOTSEQ field in the reset configuration word high register (RCWH). If the boot sequencer mode is selected, the I^2C module communicates with one or more EEPROM through the I^2C interface to initialize one or more configuration registers of the PowerQUICC II Pro. For the complete data format for programming the I^2C EEPROM, see *MPC8308 PowerQUICC II Pro Processor Reference Manual*.

The boot sequencer contains a basic level of error detection. If the I^2C boot sequencer fails while loading the reset configuration words are loaded, the RSR[BSF] bit is set. If a preamble or CRC fail is detected in boot sequencer mode, there is no internal or external indication that the boot sequencer operation failed. It is recommended to set aside a GPIO pin for error signaling purpose.

5.5 $\overline{\text{HRESET}}$

The $\overline{\text{HRESET}}$ signal is not a pure input signal. It is an open-drain signal that the MPC8308 processor can drive low. The connection on the left side of this figure causes signal contention and must not be used.

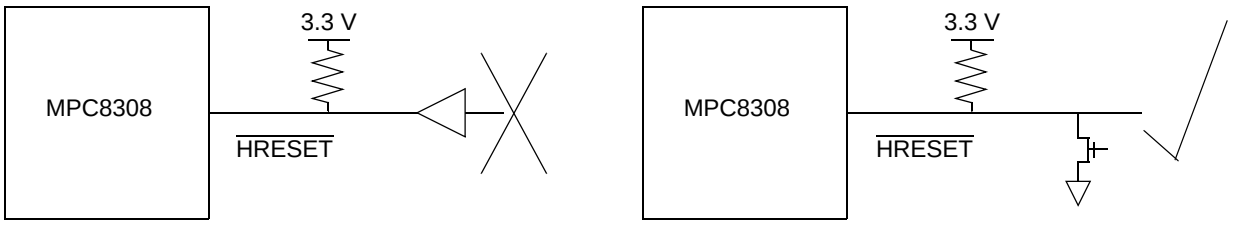


Figure 6. $\overline{\text{HRESET}}$ Connection

6 JTAG and Debug

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 8. Care must be taken to ensure that these pins are maintained at a valid negated state under normal operating conditions as most have asynchronous behavior and spurious assertion can cause unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE® Std 1149.1 specification, but it is provided on all processors that implement the Power Architecture™. The device requires $\overline{\text{TRST}}$ to be asserted during power-on reset flow to ensure that the JTAG boundary logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert $\overline{\text{TRST}}$ during the power-on reset flow. Simply tying $\overline{\text{TRST}}$ to $\overline{\text{PORESET}}$ is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to assert $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ independently to control the processor fully. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 8 allows the COP port to assert $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ independently, while ensuring that the target can drive $\overline{\text{PORESET}}$ as well.

The COP interface has a standard header, shown in Figure 7, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter- clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in Figure 7 is common to all known emulators.

If the JTAG interface and COP header are not used, Freescale recommends all of the following connections:

- $\overline{\text{TRST}}$ should be tied to $\overline{\text{PORESET}}$ through a 0 kΩ isolation resistor so that it is asserted when the system reset signal ($\overline{\text{PORESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 8. If this is not possible, the isolation resistor allows future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.
- No pull-up/pull-down is required for TDI, TMS, TDO, or TCK.

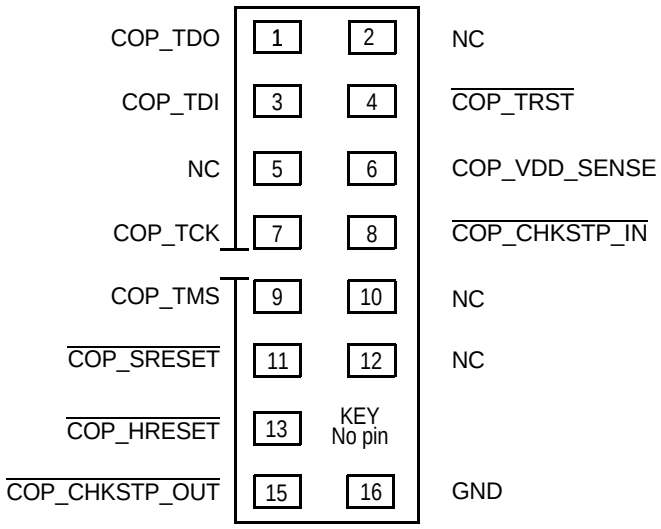
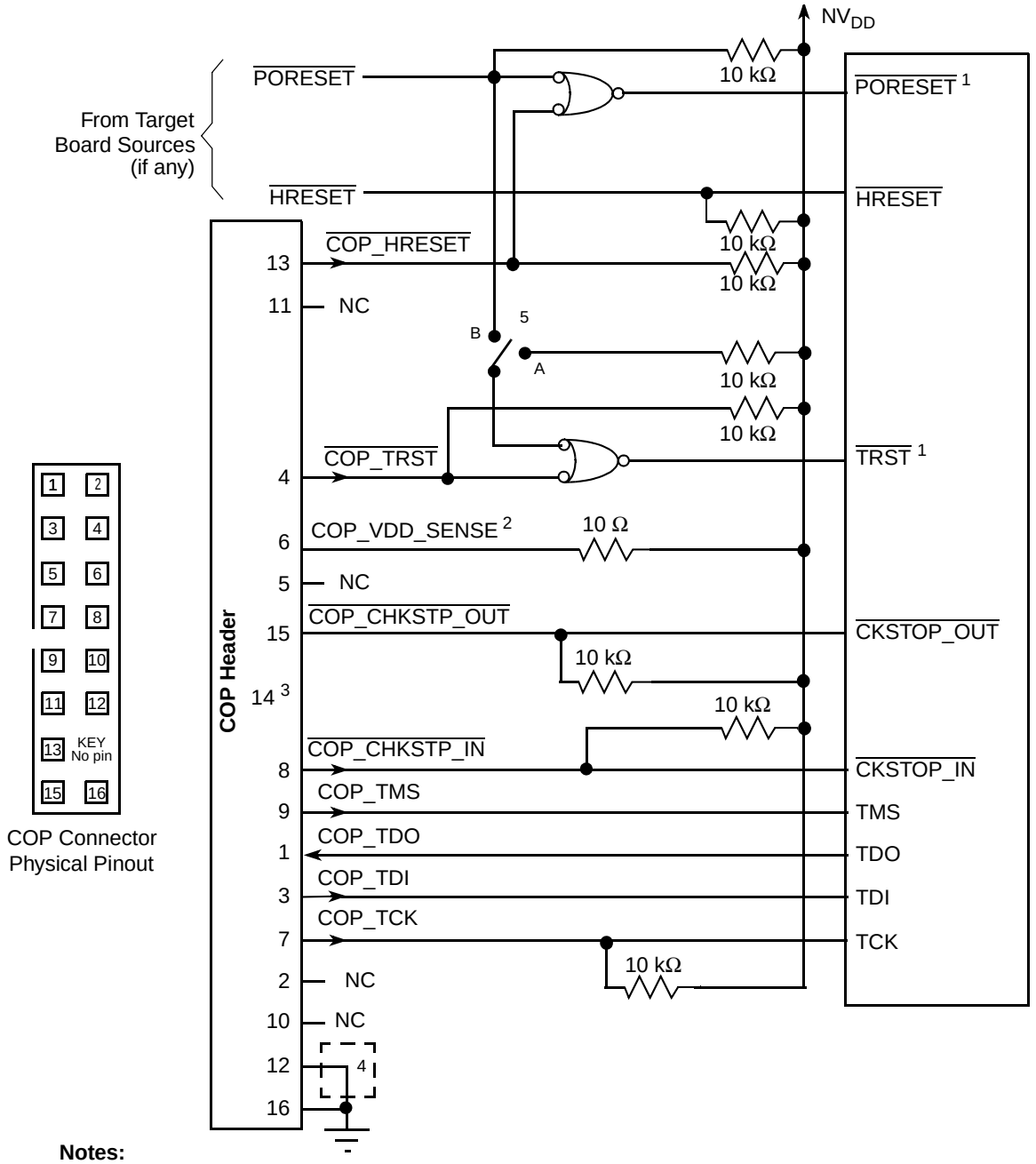


Figure 7. COP Connector Physical Pinout



Notes:

1. The COP port and target board should be able to assert $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ independently to the processor to control the processor fully as shown here.
2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the /TRST line. If BSDL testing is not being performed, this switch should be closed to position B.

Figure 8. JTAG Interface Connection

This table details the termination recommendations for the JTAG, TEST, PMC, and thermal management pins.

Table 5. JTAG and TEST Pin Listing

Signal	Pin Type	Termination		Notes
		If used	If not used	
TCK	I	As needed + 10 kΩ to NV_{DD}	10 kΩ to NV_{DD}	Commonly used for boundary scan testing.
TDI	I	As needed	Open	This JTAG pin has a weak internal pull-up P-FET that is always enabled.
TDO	O	As needed	Open	Actively driven during RESET
TMS	I	As needed	Open	This JTAG pin has a weak internal pull-up P-FET that is always enabled.
$\overline{\text{TRST}}$	I	Tie to the output of a Negative OR gate	Tie to $\overline{\text{PORESET}}$ through a 0 Ω	This JTAG pin has a weak internal pull-up P-FET that is always enabled. If an In-Circuit Emulator is used in the design, $\overline{\text{TRST}}$ should be tied to the output of a Negative OR gate logic. The inputs to the Negative OR gate logic should be any external $\overline{\text{TRST}}$ source and the $\overline{\text{PORESET}}$ signal
Test				
TEST_MODE	I	Tie directly to GND		—
DEBUG				
$\overline{\text{QUIESCE}}$	O	As needed	Open	—
Thermal Management				
THERM0	I	As needed	Tie to GND	Thermal sensitive resistor

7 Functional Blocks

This section presents the recommendations and guidelines for designing with various functional blocks on the MPC8308.

7.1 DDR2 SDRAM

Refer to the following application notes for details on layout consideration and DDR programming guidelines:

- AN2910: *Hardware and Layout Design Considerations for DDR2 Memory Interfaces,* for signal integrity and layout considerations.
- AN3369: *PowerQUICC™ III DDR2 SDRAM Controller Register Setting Considerations,* for DDR programming guidelines.

The DDR controller on the PowerQUICC II Pro can be configured with a 32- or 16-bit data bus interface. The DDR_SDRAM_CFG[DBW] bit controls the bus width selection. For details on these register settings, see *MPC8308 PowerQUICC II Pro Processor Reference Manual*.

This table lists the DDR SDRAM pins.

Table 6. DDR SDRAM Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
MDQ[0:31]	I/O	As needed	Open	When in use, proper signal integrity analysis must be performed using the respective device IBIS model. Parallel termination is optional for DDR signals and should be simulated to verify necessity.
MECC[0:7]	I/O	As needed	Open	When in use, proper signal integrity analysis must be performed using the respective device IBIS model. Parallel termination is optional for DDR signals and should be simulated to verify necessity.
MDM[0:3], MDM[8]	O	As needed	Open	
MDQS[0:3], MDQS[8]	I/O	As needed	Open	In 16 bit mode, unused MDQS pin should be grounded with 150Ω resistor
MBA[2:0]	O	As needed	Open	—
MA[13:0]	O	As needed	Open	—
$\overline{\text{MWE}}$	O	As needed	Open	—
$\overline{\text{MRAS}}$	O	As needed	Open	—
$\overline{\text{MCAS}}$	O	As needed	Open	—
$\overline{\text{MCS}}$[0:1]	O	As needed	Open	—

Table 6. DDR SDRAM Pin Listing (continued)

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
MCKE	O	As needed	Open	This output is actively driven during reset rather than being three-stated during reset.
MCK[0:2]	O	As needed	Open	—
$\overline{\text{MCK[0:2]}}$	O	As needed	Open	—
MODT[0:1]	O	As needed	Open	—

7.2 Enhanced Local Bus Controller

The eLBC provides one GPCM, one FCM, and three UPMs for the local bus, with no restriction on how many of the four banks (chip selects) can be programmed to operate with any given machine. When a memory transaction is dispatched to the eLBC, the memory address is compared with the address information if each bank. The corresponding machine assigned to that bank (GPCM, FCM, or UPM) then takes ownership of the external signals that control the access and maintains control until the transaction ends. Thus, with the eLBC in GPCM or FCM, or UPM mode, only one of the four chip selects is active at any time for the duration of the transaction.

The local bus clock is not configured while it is executing from the local bus, but rather by executing code from the DDR. The address and data buses are non-multiplexed.

7.2.1 Local Bus Data and Address

This table lists guidelines for connecting to 8-bit, and 16-bit devices. LA[0] is the most significant address bit, and LA[25] is the least significant address bit. LD[0] is the most significant data bit and LD[15] is the least significant data bit. Notice that for a 16-bit port connection, the address LA[25] is normally not required because byte lane control is achieved through signals as listed in this table.

Table 7. Local Bus Byte Lane Control

Device Data Width	Address	Data	Byte Lane Control		
			GPCM	FCM	UPM
8-bit	LA[0:25]	LD[0:7]	$\overline{\text{LWE}}$[0]	LFWE	$\overline{\text{LBS}}$[0]
16-bit	LA[0:24]	LD[0:15]	$\overline{\text{LWE}}$[0:1]	—	$\overline{\text{LBS}}$[0:1]

7.2.2 NAND Flash Interface

The FCM provides a glueless interface to parallel-bus NAND flash EEPROM devices. The figure given below shows a simple connection between an 8-bit port size NAND flash EEPROM and the eLBC in FCM mode. Commands, address bytes and data are all transferred on LD[0:7].

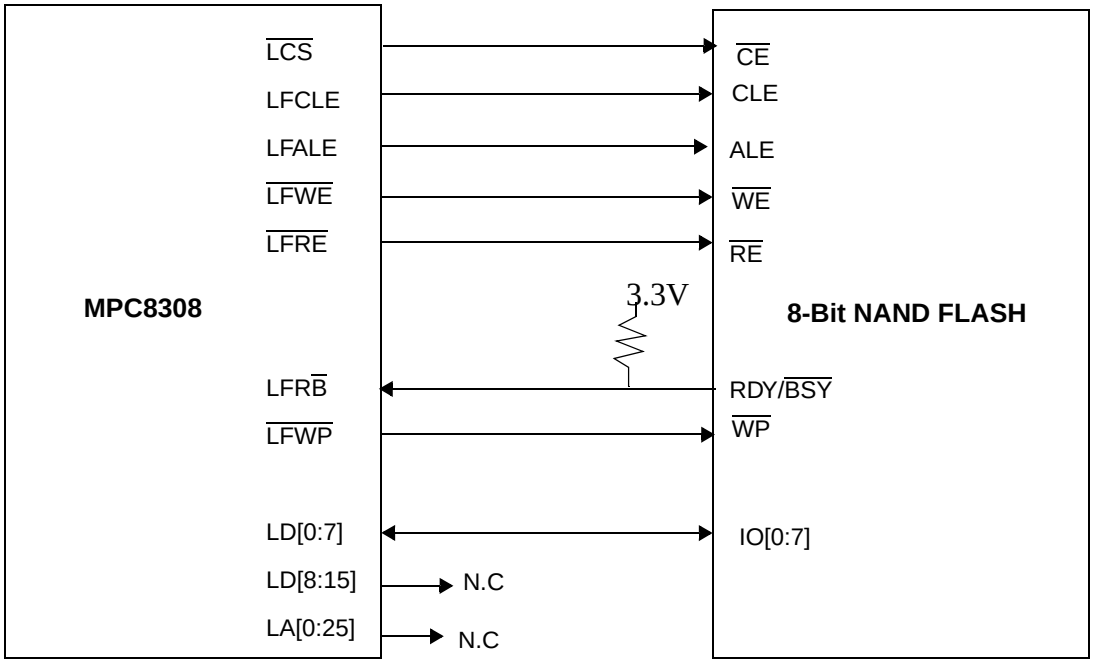


Figure 9. NAND Flash Connection Diagram

This table lists the local bus pins.

Table 8. Local Bus Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
LD[0:15]	I/O	As needed	Open	—
LA[0:25]	O	As needed	Open	—
$\overline{\text{LCS}}$[0:3]	O	As needed	Open	—
$\overline{\text{LWE0}}$/$\overline{\text{LFWE0}}$/ $\overline{\text{LBS0}}$	O	As needed	Open	—
$\overline{\text{LWE1}}$/ $\overline{\text{LBS1}}$	O	As needed	Open	—
LBCTL	O	As needed	Open	—
LGPL0/LFCLE	O	As needed	Open	—
LGPL1/LFALE	O	As needed	Open	—
LGPL2/$\overline{\text{LFRE}}$/$\overline{\text{LOE}}$	O	As needed	Open	—
LGPL3/$\overline{\text{LFWP}}$	O	As needed	Open	—
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/ $\overline{\text{LFRB}}$	I/O	As needed	Open	Output when configured as LGPL4.

Table 8. Local Bus Pin Listing (continued)

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
LGPL5	O	As needed	Open	—
LCLK0	O	As needed	Open	—

7.3 Universal Serial Bus (USB)

This figure shows the USB interface block diagram.

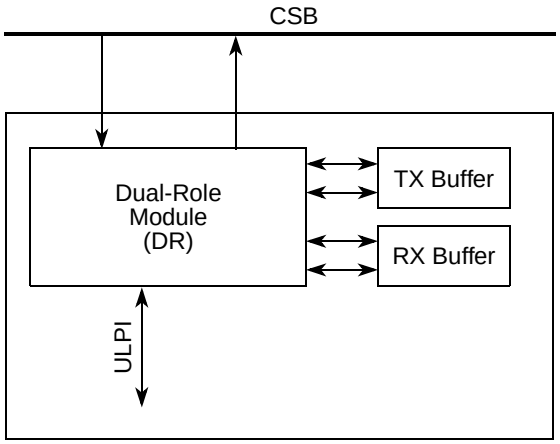


Figure 10. USB Interface Block Diagram

The USB DR module is a USB 2.0-compliant serial interface engine for implementing a USB interface. The DR controller can act as a device or host controller. Interfaces to negotiate the host or device role on the bus in compliance with the on-the-go (OTG) supplement to the USB specification are also provided. The DR module supports the required signaling for UTMI low pin count interface (ULPI) transceivers (PHYs). The PHY interfacing to the ULPI is an external PHY.

The USB DR module has three basic operating modes: host, device, and OTG. This table lists the ULPI pins.

Table 9. ULPI Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
USBDR_TXDRXD[0:7]	I/O	As needed	Open	Pin functionality determined by SICRH[12-13] bit setting
USBDR_CLK	I	As needed	1 kΩ to GND	Pin functionality determined by SICRH[12-13] bit setting

Table 9. ULPI Pin Listing (continued)

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
USBDR_NXT	I	As needed	1 kΩ to GND	Pin functionality determined by SICRH[12-13] bit setting
USBDR_DIR	I	As needed	1 kΩ to GND	Pin functionality determined by SICRH[12-13] bit setting
USBDR_STP	O	As needed	Open	Pin functionality determined by SICRH[12-13] bit setting
USBDR_PWR_FAULT	I	As needed	1 kΩ to GND	Pin functionality determined by SICRH[12-13] bit setting
USBDR_PCTL[0:1]	O	As needed	Open	Pin functionality determined by SICRH[12-13] bit setting

7.4 Integrated Programmable Interrupt Controller (IPIC)

The integrated programmable interrupt controller (IPIC) provides interrupt management for receiving hardware-generated interrupts from internal and external sources. It also prioritizes and delivers the interrupts to the CPU for servicing. The $\overline{\text{IRQ}}$ lines are multiplexed with signals CKSTOP_IN and CKSTOP_OUT interface pins. The configuration of each $\overline{\text{IRQ}}$ pin is programmed using the system I/O configuration low register (SICRL). This table lists the programmable interrupt controller pins.

Table 10. Programmable Interrupt Controller Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
$\overline{\text{IRQ}}$[0]/$\overline{\text{MCP\_IN}}$	I	As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	—
$\overline{\text{IRQ}}$[1]/$\overline{\text{MCP\_OUT}}$	I/O	As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	—
$\overline{\text{IRQ2}}$/CKSTOP_OUT	I/O	As needed + 2k–10k to NV_{DD}	2k–10k to NV_{DD}	Pin functionality determined by SICRL[6–7] bit setting.
$\overline{\text{IRQ3}}$/CKSTOP_IN	I	As needed + 2k–10k to NV_{DD}	2k–10k to NV_{DD}	Pin functionality determined by SICRL[6–7] bit setting.

7.5 Enhanced Three-Speed Ethernet Controllers (eTSECs)

The two enhanced three-speed Ethernet controllers (eTSECs) support 10, 100, and 1000 Mbps Ethernet/802.3 networks. The complete eTSEC is designed for single MAC applications with standard MAC-PHY interfaces to connect to an external Ethernet transceiver:

- IEEE 802.3, 802.3u, 802.3x, 802.3z, 802.3ac, 802ab compliant
- 10/100 Mbps IEEE 802.3 MII
- 10/100 Mbps RGMII
- 1000 Mbps full-duplex RGMII

Two eTSECs can be independently configured to support any one of these interfaces. The reset configuration word high controls the hardware configuration of the two eTSEC MAC-PHY interfaces. RCWH[TSEC1M] and RCWH[TSEC2M] are used to configure eTSEC1 and eTSEC2, respectively, in either MII or RGMII mode.

eTSEC1 interface pins are multiplexed with reset configuration source signals. Some eTSEC2 interface pins are multiplexed with GPIO pins.

This table lists the pin usage and software configuration for each particular MAC-PHY mode.

Table 11. eTSEC MAC-PHY Modes

	MII	RGMII
TSECn_GTX_CLK125	—	125 MHz clock
TSEC*n*_COL	COL	—
TSEC*n*_CRS	CRS	—
TSEC*n*_GTX_CLK	—	GTX_CLK
TSEC*n*_RX_CLK	RX_CLK	RX_CLK
TSEC*n*_RX_DV	RX_DV	RX_CTL
TSEC*n*_RX_ER	RX_ER	—
TSEC*n*_RXD[3:0]	RxD[3:0]	RxD[3:0]
TSEC*n*_TX_CLK	TX_CLK	—
TSEC*n*_TXD[3:0]	TxD[3:0]	TxD[3:0]
TSEC*n*_TX_EN	TX_EN	TX_CTL
TSEC*n*_TX_ER	TX_ER	—
Software configuration	RCWH[TSEC*n*M] = 000 MACCFG2[22–23] = 10	RCWH[TSEC*n*M] = 011 MACCFG2[22–23] = 10

The two eTSECs have a common management interface that controls all external PHYs. This table lists the eTSEC pins.

Table 12. Enhanced Three-Speed Ethernet Controller Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
TSEC_MDC	O	As needed	Open	—
TSEC_MDIO	I/O	As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	—
TSEC*n*_GTX_CLK125/ TSEC*n*_TX_CLK	I	125 MHz clock (RGMII mode) Or 25 MHz clock (MII mode)	1 kΩ to GND	—
TSEC*n*_COL	I/O	As needed	1 kΩ to GND	—
TSEC*n*_CRS	I/O	As needed	1 kΩ to GND	—
TSEC*n*_GTX_CLK	O	As needed	1 kΩ to GND	—
TSEC*n*_RX_CLK	I	As needed	1 kΩ to GND	—
TSEC*n*_RX_DV	I	As needed	1 kΩ to GND	—
TSEC*n*_RX_ER	I	As needed	1 kΩ to GND	—
TSEC*n*_RXD[3:0]	I	As needed	1 kΩ to GND	—
TSEC*n*_TXD[3:0]	O	As needed	Open	—
TSEC*n*_TX_EN	O	As needed	Open	—
TSEC*n*_TX_ER	O	As needed	Open	—

NOTE

eTSEC1 pin functionality is determined by SICRL[24–25] bit settings and eTSEC2 pin functionality is determined by SICRH[6–7], SICRH[8–9], and SICRH[18–19] bit settings.

7.6 SerDes PHY (PCI Express Interface)

The SerDes PHY block operates as a ×1 PCI Express link at 2.5 Gbps. This table lists the pins and the implementation notes.

Table 13. SerDes Pin List

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
TXA	O	As needed	Open	Differential signal, serial transmitter, lane A, positive data
$\overline{\text{TXA}}$	O	As needed	Open	Differential signal, serial transmitter, lane A, negative data
RXA	I	As needed	Connect to GND	Differential signal, serial receiver, lane A, positive data
$\overline{\text{RXA}}$	I	As needed	Connect to GND	Differential signal, serial receiver, lane A, negative data
SD_REF_CLK	I	As needed	Connect to GND	PCI Express: 100 MHz differential clock must be connected.
$\overline{\text{SD\_REF\_CLK}}$	I	As needed	Connect to GND	PCI Express: 100 MHz differential clock must be connected.
SD_IMP_CAL_TX	I	As needed:	Connect to 1 V	High: Fixed Impedance Low: Impedance can be calibrated
SD_IMP_CAL_RX	I	As needed:	Connect to 1 V	High: Fixed Impedance Low: Impedance can be calibrated
SD_PLL_TPD	O	Open	Open	Test point
SD_PLL_TPA_ANA	O	Open	Open	—

This figure shows the connection diagram for the impedance calibration pins.

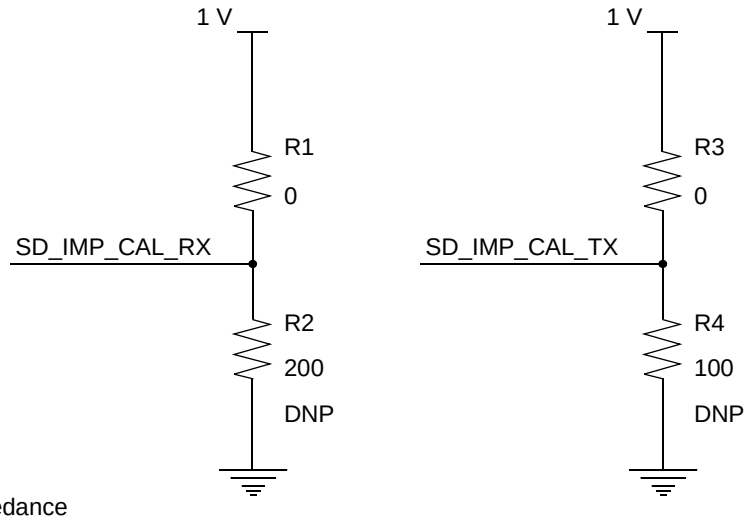


Figure 11. Connection Diagram for Impedance Calibration Pins

7.6.1 PCI Express Layout Guidelines

The PCI Express layout guidelines are described as follows:

- Recommended microstrip trace routing guidelines
  - — Single ended: 50 Ω +/– 15%
  - — Differential: 100 Ω +/– 15%
- Recommended stripline trace routing guidelines
  - — Single ended: 50 Ω +/– 15%
  - — Differential: 100 Ω +/– 15%
- Recommended length matching intra-pair: Maximum 5 mil delta, matching maintained segment to segment, and matching at point of discontinuity. However, avoid tight bends.
- Recommended for all differential signal pairs: Maintain ≥ 20 mil trace edge to plane edge gap.
- Gnd referenced signals is recommended.
- Use Gnd stitching vias by signal layer vias for layer changes.
- Do not route over plane splits or voids. Allow no more than a half trace width routed over via antipad.
- Via usage: Limit via usage to 4 vias per TX trace and 2 vias per RX trace (6 vias total, entire path).
- Bends: Match left/right turn bends whenever possible. No 90-degree bends or tight bend structures.
- The reference clock signal pair should maintain the same reference plane for the entire routed length and should not cross any plane splits (breaks in the reference plane).
- A minimum separation from the reference clock and other traces should be maintained. Assuming a trace width of 'w', no other trace or signal should be allowed within '3w'.
- The reference clock signal pair routing length should be minimized.

- The reference clock signal pair via count should be minimized. As a rule of thumb, via count should not exceed four.
- Reference clock terminating components should be placed as close as possible to their respective devices, ideally within 100 mils of the clock/receiver component pin.
- Match all segment lengths between differential pairs along the entire length of the pair.
- Maintain constant line impedance along the routing path by keeping the same line width and line separation.
- Avoid routing differential pairs adjacent to noisy signal lines or high speed switching devices, such as clock chips.
- Keep clock lines adequately separated from I/O lines.
- Recommended PCI Express reference clock positive to PCI Express reference clock negative length matching to within 25 mils.
- Unused PCI Express clock outputs (unpopulated down devices or unpopulated add-in card connectors) should be disabled to limit EMI radiations and possible signal reflections.
- Decoupling capacitors: Several PCB-mounted 0.1 to 1.0 μF capacitors should be placed near the PCI Express silicon on the sides of the package to which the PCI Express I/O buffers connect.
- AC coupling capacitors:
  - Do not use capacitor-packs (C-packs) for PCI Express AC coupling capacitor purpose.
  - The same package size and value of capacitor should be used for each signal in a differential pair.
  - Locate capacitors for coupled traces in a differential pair at the same location along the differential traces. Place them as close to each other as possible, as allowed by DFM rules.
  - The breakout into and out of the capacitor mounting pads should be symmetrical for both signal lines in a differential pair.
- Test points and probing structures should not introduce stubs on the differential pairs.

7.7 DUART

This table lists the dual UART pins.

Table 14. Dual UART Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
UART_SOUT1/ MSRCID0/LSRCID0	O	As needed	Open	Pin functionality determined by SICRL[4–5] bit setting
UART_SIN1/ MSRCID1/LSRCID1	I	As needed	2 k–10 kΩ to NV_{DD}	Pin functionality determined by SICRL[4–5] bit setting

Table 14. Dual UART Pin Listing (continued)

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
UART_SOUT2/ MSRCID2/LSRCID2	O	As needed	Open	Pin functionality determined by SICRL[4–5] bit setting
UART_SIN2/ MSRCID3/LSRCID3	I	As needed	2 k–10 kΩ to NV_{DD}	Pin functionality determined by SICRL[4–5] bit setting

7.8 I^2C Interface

This table lists the I^2C pins.

Table 15. I^2C Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
IIC_SCL1	I/O	As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	Open-drain signal
IIC_SDA1	I/O	As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	Open-drain signal
$\overline{\text{IIC\_SCL2/ CKSTOP\_IN}}$	I/O	As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	• Open-drain signal • Pin functionality determined by SICRL[10–11] setting.
$\overline{\text{IIC\_SDA2/ CKSTOP\_OUT}}$	I/O	As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	• Open-drain signal • Pin functionality determined by SICRL[10–11] setting.

7.9 SPI

This table lists the SPI pins.

Table 16. SPI Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
SPIMOSI/ MSRCID4/ LSRCID4	I/O	**SPI:** As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	• Software configurable open-drain signal using SPMODE[OD] bit. Pull-up required only if configured as open drain. • Pin functionality determined by SICRL[2–3] bit setting.
SPIMISO/ MDVAL/ LDVAL	I/O	**SPI:** As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	• Software configurable open-drain signal using SPMODE[OD] bit. Pull-up required only if configured as open drain. • Pin functionality determined by SICRL[2–3] bit setting.
SPICLK	I/O	As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	Software configurable open-drain signal using SPMODE[OD] bit. Pull-up required only if configured as open-drain.
SPISEL	I	As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	Should be used when SPI configured as Slave.

7.10 eSDHC

This table lists the eSDHC interface pins.

Table 17. eSDHC Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
SD_CLK	O	As needed	Open	Pin functionality determined by SICRH[0–1] bit setting
SD_CMD	I/O	As needed + 10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	Pin functionality determined by SICRH[0–1] bit setting
SD_DAT3	I/O	As needed + 100 kΩ to GND	2 k–10 kΩ to NV_{DD}	• Can function as DAT3 line or as card detection pin in 4-bit mode and as card detection pin in 1-bit mode • Pin functionality determined by SICRH[4–5] bit setting
SD_DAT2	I/O	As needed + 10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	• Can function as DAT2 line or as read wait in 4-bit mode and as read wait in 1-bit mode • Pin functionality determined by SICRH[4–5] bit setting
SD_DAT1	I/O	As needed + 10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	• Can function as DAT1 line or as interrupt detect in 4-bit mode and as read wait in 1-bit mode • Pin functionality determined by SICRH[2–3] bit setting

Table 17. eSDHC Pin Listing (continued)

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
SD_DAT0	I/O	As needed + 10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	• Can function as DAT0 line or as interrupt detect • Pin functionality determined by SICRH[2–3] bit setting
$\overline{\text{SD\_CD}}$	I	As needed + 100 kΩ to NV_{DD} on the $\overline{\text{SD\_CD}}$ signal and a 330 Ω pull down on the common pin of the WP/CD Switch of the SD Card connector	2 k–10 kΩ to NV_{DD}	• $\overline{\text{SD\_CD}}$ low implies card is present and high implies card is absent. • Pin functionality determined by SICRH[0–1] bit setting
SD_WP	I	As needed + 100 kΩ to NV_{DD} on the SD_WP signal and a 330 Ω pull down on the common pin of the WP/CD Switch of the SD Card connector	2 k–10 kΩ to NV_{DD}	• SD_WP high implies write protection is enabled on the SD Card and low implies write protection is disabled on the SD Card • Pin functionality determined by SICRH[0–1] bit setting

7.11 PMC

The e300 core can be programmed to go into a Nap mode or Sleep mode to save dynamic power. The nap mode can be exited according to the internal time base unit of the core or any external interrupt assertion. The sleep mode can be exited only on assertion of any interrupt to the core. This table lists the PMC pins.

Table 18. PMC External Signal

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
$\overline{\text{QUIESCE}}$	O	As needed	Open	Status Pin. Asserted low when core enters sleep/nap mode.

8 Revision History

This table provides a revision history for this document.

Table 19. Document Revision History

Rev. Number	Date	Substantive Change(s)
1	11/2011	• Modified the second line of first para in Section 2.6, “PLL Power Supply Filtering”, to read as, “The AV_{DD} level should be derived directly from VDD through a low frequency filter scheme.” • In Figure 2, removed 0.01µF capacitor. • In Figure 3, changed the resistor from 10Ω to 1Ω and changed the capacitor from 0.01µF to 3nF. • In Figure 4, RTC block is added. • In Table 2, updated the ‘connection’ column for ‘NV_{DD}’ to 3.3 V ± 300 mV. • In Table 3, added a row for RTC_PIT_CLOCK. • In Table 6, updated MDQS[0:3] pin note information to read as: “In 16 bit mode, unused MDQS pin should be grounded with 150Ω resistor”. • In Table 12, replaced the ‘connection’ column for TSEC_MDIO from LV_{DD1} to NV_{DD} and removed the note ‘Open drain signal’. • Section 7.11, “PMC”, updated first paragraph.
0	06/2010	Initial public release

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